

WHAT IS CLAIMED IS:

1. A method of simulating an operation of a memory, comprising the steps of:

simulating a read/write operation corresponding to a location specified by a first bit set of a memory address including a plurality of bits, using a memory model describing the operation of the memory; and

generating an error in the read/write operation of the memory model in accordance with a value of a second bit set of the memory address by making a change to one of write data to be written to the memory model and read data read therefrom, the second bit set being not used for the simulation of the read/write operation using the memory model.

2. The method according to claim 1, wherein the second bit set of the memory address includes error address information for specifying an error generating address and error mode information for specifying a content of error generation, and the error generating step comprises:

a step of detecting whether a value of the first bit set of the memory address and a value specified by the error address information coincide with each other; and

a step of reversing at least one bit of one of the write data and the read data in accordance with the error mode information when the value of the first bit

set and the value specified by the error address information coincide with each other.

3. The method according to claim 1, wherein the memory model describes an operation of a nonvolatile semiconductor memory to which write data and an error correction code thereof are written in units of data size so as to correspond to each other, and the method further comprises a step of simulating an error correcting operation of a memory controller for controlling the nonvolatile semiconductor memory, based on the read data and the error correction code, using an LSI model describing an operation of the memory controller.

4. The method according to claim 3, wherein the error generating step includes a first error mode for making a change to one of the write data to be written to the memory model and the read data read therefrom within the number of error correctable bits using the error correction code and a second error mode for making a change thereto by the number of bits exceeding the number of error correctable bits, one of the first error mode and the second error mode being chosen in accordance with the value of the second bit set of the memory address.

5. A method of simulating an operation of a memory, comprising the steps of:

simulating a read/write operation corresponding to

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6. A system for simulating an operation of

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address information for specifying an error generating address and error mode information for specifying a content of error generation, and the error generating means comprises:

5 means for detecting whether a value of the first bit set of the memory address and a value specified by the error address information coincide with each other; and

10 means for reversing at least one bit of one of the write data and the read data in accordance with the error mode information when the value of the first bit set and the value specified by the error address information coincide with each other.

15 8. The system according to claim 6, wherein the memory model describes an operation of a nonvolatile semiconductor memory to which write data and an error correction code thereof are written in units of data size so as to correspond to each other, and the system further comprises means for simulating an error
20 correcting operation of a memory controller for controlling the nonvolatile semiconductor memory, based on the read data read from the memory model and the error correction code, using an LSI model describing an operation of the memory controller.

25 9. The system according to claim 8, wherein the error generating means includes a first error mode for making a change to one of the write data to be written

to the memory model and the read data read therefrom within the number of error correctable bits using the error correction code and a second error mode for making a change thereto by the number of bits exceeding the number of error correctable bits, one of the first error mode and the second error mode being chosen in accordance with the value of the second bit set of the memory address.

10. A system for simulating an operation of a memory, comprising:

memory model means having a memory address space which is to be specified by a lower bit set of a memory address including a plurality of bits, the memory address corresponding to a memory address space of the memory, for simulating a read/write operation corresponding to a location specified by the lower bit set of the memory address; and

error generating means to which a higher bit set of the memory address is supplied, for generating an error in the read/write operation of the memory model means in accordance with a value of the higher bit set of the memory address by making a change to one of write data to be written to the memory model means and read data read therefrom.

11. A recording medium having stored thereon a computer readable program for simulating an operation of a memory, the program comprising:

first code means for simulating a read/write operation corresponding to a location specified by a first bit set of a memory address including a plurality of bits, using a memory model describing the operation of the memory; and

second code means for generating an error in the read/write operation of the memory model by making a change to one of write data to be written to the memory model and read data read therefrom in accordance with a value of a second bit set of the memory address, the second bit set being not used for the simulation using the memory model.

12. The storage medium according to claim 11, wherein the second bit set of the memory address includes error address information for specifying an error generating address and error mode information for specifying a content of error generation, and the second code means comprises:

means for detecting whether a value of the first bit set and a value specified by the error address specifying information coincide with each other; and

means for reversing at least one bit of one of the write data and the read data in accordance with the error mode information when the value of the first bit set and the value specified by the error address specifying information coincide with each other.

13. The recording medium according to claim 11,

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first code means for simulating a read/write operation corresponding to a location specified by

